ABSTRACT OF THE DISCLOSURE

There is disclosed a phase detector and phase locked loop circuit in which a maximum operation frequency is high. The phase detector of the present invention comprises three S-R flip-flops each of which comprises two NAND gates, a NAND gate connected to an input terminal of the S-R flip-flop, and an inverter. Even when a phase difference between a reference clock signal and a clock signal is large, UP and DOWN signals can be outputted in accordance with the phase difference between both signals, and therefore the maximum operation frequency can be set to be higher than that of a conventional phase detector.